Page 7, delete the whole paragraph starting in line 11 and replace it with the following new paragraph:

According to the present invention, active hydrogen nitride radicals NH* are formed efficiently by activating NH_3 or a mixed gas of N_2 and H_2 in microwave exited plasma of Ar or Kr. By causing the hydrogen nitride radicals NH_3* to react, it becomes possible to form a silicon nitride film having a quality superior to a silicon thermal oxide film formed at about 1000°C on the (111) surface of a Si crystal at a low temperature of 550°C or less. The silicon nitride film thus formed can be used as a high-dielectric gate insulation film and it becomes possible to form a high-performance semiconductor device or a high-performance semiconductor integrated circuit device on the (111) surface of the Si crystal. It should be noted that the (111) surface of the Si crystal may be the one defining the principal surface of a Si single crystal substrate or the one formed in a part thereof. Further, the (111) surface may be the one appearing at the surface of a polysilicon film.

Page 12, delete the whole paragraph starting in line 28 and replace it with the following new paragraph:

FIG. 2 shows the thickness of the oxide film for the case in which the total pressure inside the processing chamber 101 is changed while maintaining the Kr and oxygen pressure ration such that the proportion of Kr is 97% and the proportion of oxygen is 3%. In the experiment of FIG. 2, it should be noted that the silicon substrate was held at 400°C and the oxidation was conducted over the duration of 10 minutes.

Page 28, delete the whole paragraph starting in line 2 and replace it with the following new paragraph:

FIGS. 10A – 10D show the fabrication process of a MIS transistor according to a first embodiment of the present invention.

Page 28, delete the whole paragraph starting in line 5 and replace it with the following new paragraph:

Referring to FIG. 10A, a stacked gate insulation film 12 is formed on a (100) principal surface or a (111) principal surface of a Si substrate 11, by depositing a Si oxide film 12A and a Si nitride film 12B with respective thicknesses of 1 nm and 2 nm by conducting the process

95 steps explained before in the substrate processing apparatus of FIG. 1. Next, in the step of FIG. 10B, a polysilicon film 13 is deposited on the stacked gate insulation film 12.

Page 28, delete the whole paragraph starting in line 14 and replace it with the following new paragraph:

96 Next, in the step of FIG. 10C, the polysilicon film 13 is patterned into a gate electrode 13A, and ion implantation process of impurity element is conducted into the Si substrate 11 while using the gate electrode 13A as a mask. As a result, LDD regions 11A and 11B are formed in the substrate 11 at both lateral sides of the gate electrode 13A.

Page 28, delete the whole paragraph starting in line 22 and replace it with the following new paragraph:

97 Next, in the step of FIG. 10D, sidewall insulation films 14A and 14B are formed on respective sidewall surfaces of the gate electrode 13A, and high-concentration diffusion regions 11C and 11D are formed in the substrate 11 at outer regions of the sidewall insulation films 14A and 14B as source and drain regions of the MIS transistor. The diffusion regions 11C and 11D are formed by conducting an ion implantation process of an impurity element while using the sidewall insulation films 14A and 14B as a mask.

Page 29, delete the whole paragraph starting in line 8 and replace it with the following new paragraph:

98 Measurement of the channel mobility conducted on the MIS transistor of FIG. 10D with regard to the surface orientation dependence of the channel mobility has revealed the fact that the channel mobility increases by the factor of about 1.2 or more in the transistor formed on the (111)-oriented Si substrate as compared with the transistor formed on the (100)-oriented Si substrate, irrespective of whether the MIS transistor is an n-channel transistor or the MIS transistor is a p-channel transistor.

Page 34, delete the whole paragraph starting in line 1 and replace it with the following new paragraph:

99 Typically, the ferroelectric film 1106 is formed by a sputtering process such that there appears a Sr: Ta: Nb of 1:0.7:0.3 in the ferroelectric film, and a plasma oxidation process is

conducted thereafter at the temperature of 400°C by carrying out the Kr/O_2 plasma oxidation processing explained before. As a result, the ferroelectric film 1106 has a composition represented as $Sr_2(Ta_{0.7}Nb_{0.3})_2O_7$.

Page 35, delete the whole paragraph starting in line 23 and replace it with the following new paragraph:

In conventional ferroelectric memory devices, the ferroelectric film 1106 of the SrTaNbO system has been formed by a sol-gel process, followed by a crystallization process conducted by a thermal annealing process at high temperature of 900°C or more. However, the ferroelectric film formed by such a conventional process has suffered from the problem of inhomogeneous film composition and deterioration of device performance that is caused by elemental diffusion associated with the use of high temperature. Further, the ferroelectric film thus formed shows a poor leakage characteristic. On the contrary, the present invention enables formation of a high-quality $Sr_2(Ta_{0.7}Nb_{0.3})_2O_7$ film characterized by the features of excellent uniformity, free from element diffusion, excellent leakage current characteristic, and the like, by accurately controlling the Sr: Ta: Nb ratio to 1:0.7:0.3 in the sputtering process of the SrTaNbO film and further by applying the Kr/O_2 plasma oxidation process at low temperature.

Page 44, delete the whole paragraph starting in line 32 and replace it with the following new paragraph:

The channel layers 1503 and 1504 are covered by an insulation film 1509, and a polysilicon gate electrode 1510 is formed on the channel layer 1503 via the insulation film 1509. Similarly, a polysilicon gate electrode 1511 is formed on the channel layer 1504 via the insulation film 1509. Further, an insulation film 1512 of SiO_2, BSG or BPSG is formed on the Si_3N_4 film 1502 so as to cover the channel layers 1503 and 1504 and further the gate electrodes 1510 and 1511, and a source electrode 1513 and a drain electrode 1514 are formed on the insulation film 1512 respectively in contact with the source region 1505 and the region 1506. It should be noted that the drain electrode 1514 function also as the source electrode of the p-MOS transistor formed on the channel layer 1504 and thus makes a contact with the source region 1507 via the insulation film 1512. Further, a source electrode 1515 of the p-MOS TFT is formed on the insulation film 1512, wherein the source electrode 1515 makes a contact with the drain region 1508 via the insulation film.